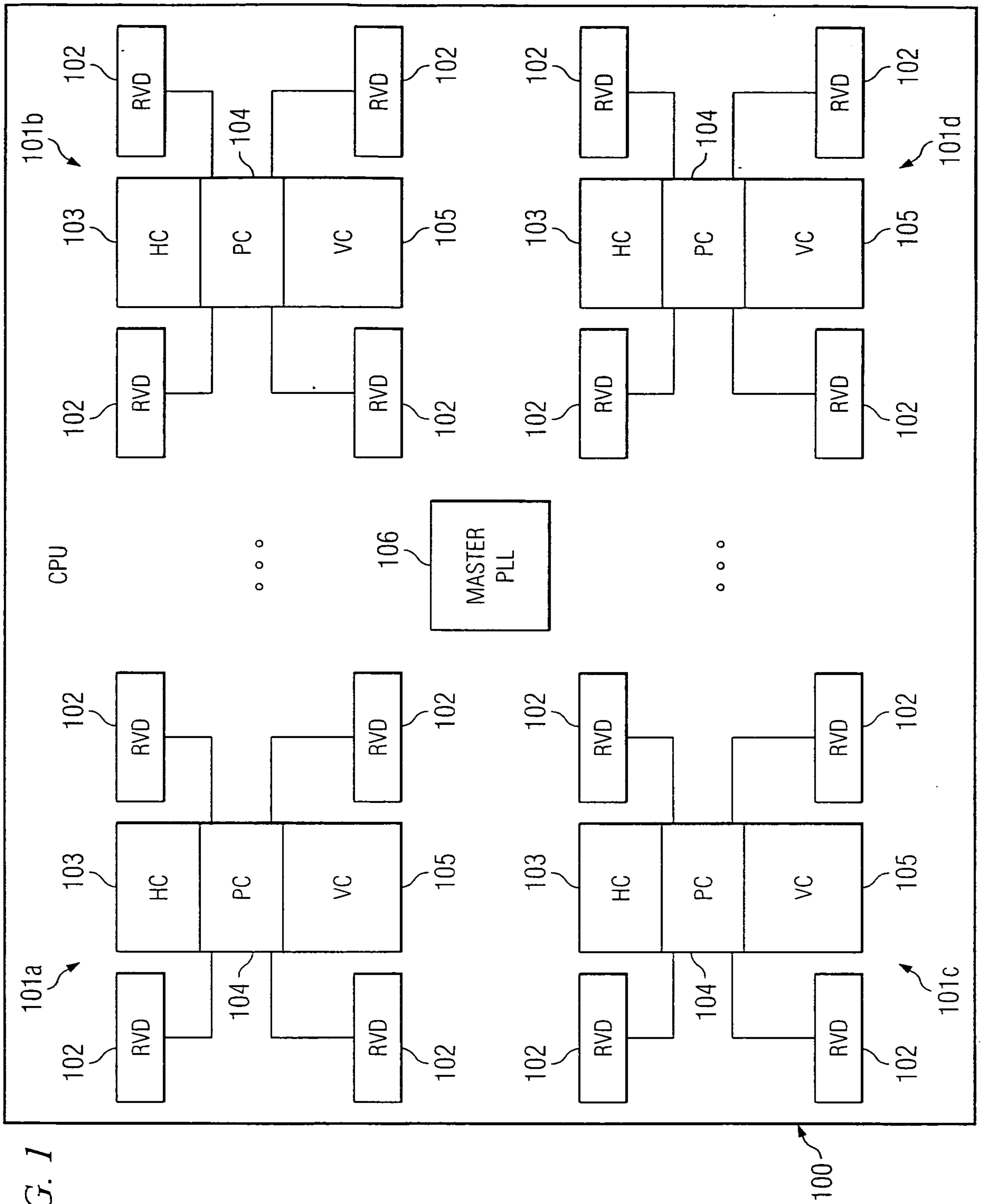

CPU
RVD
HC
PC
VC
MASTER PLL

FIG. 1

FIG. 2

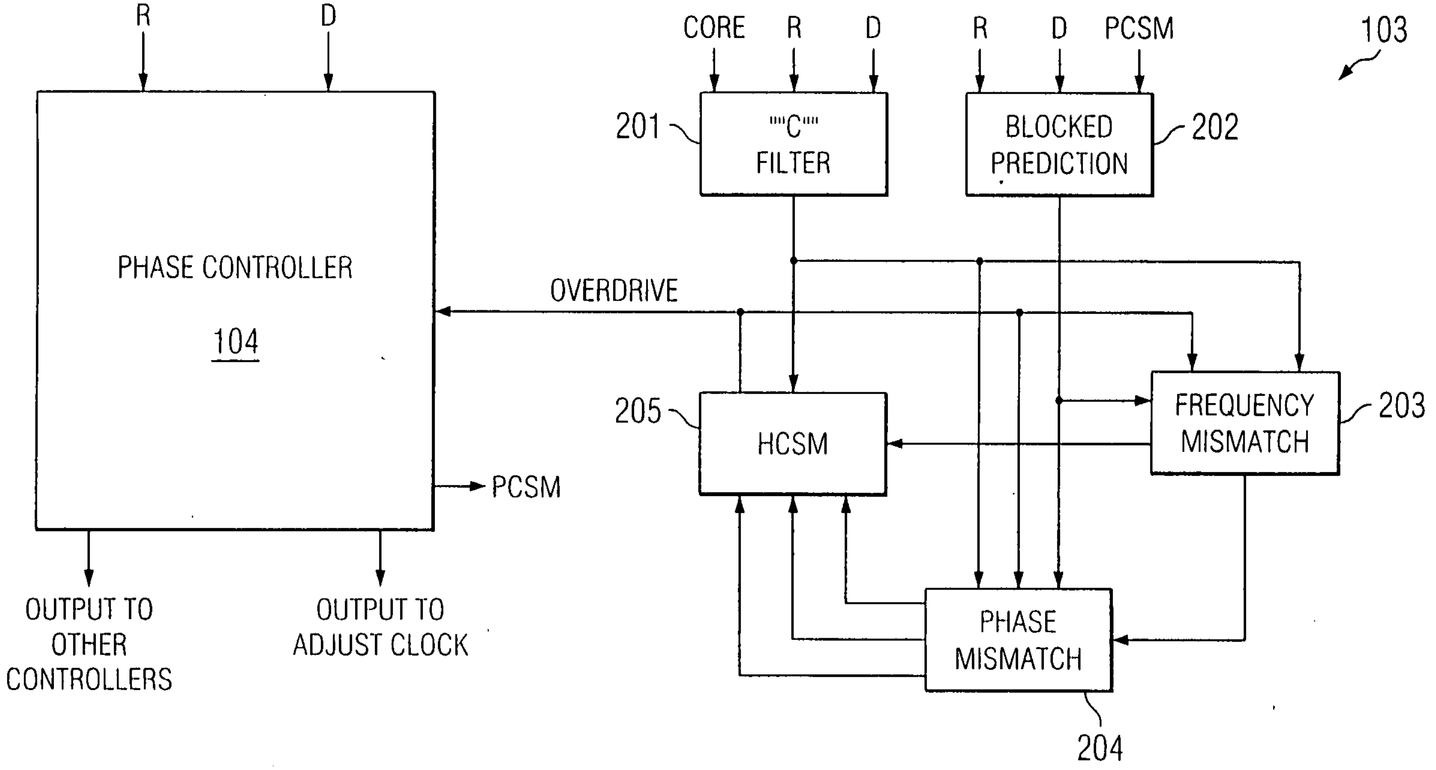
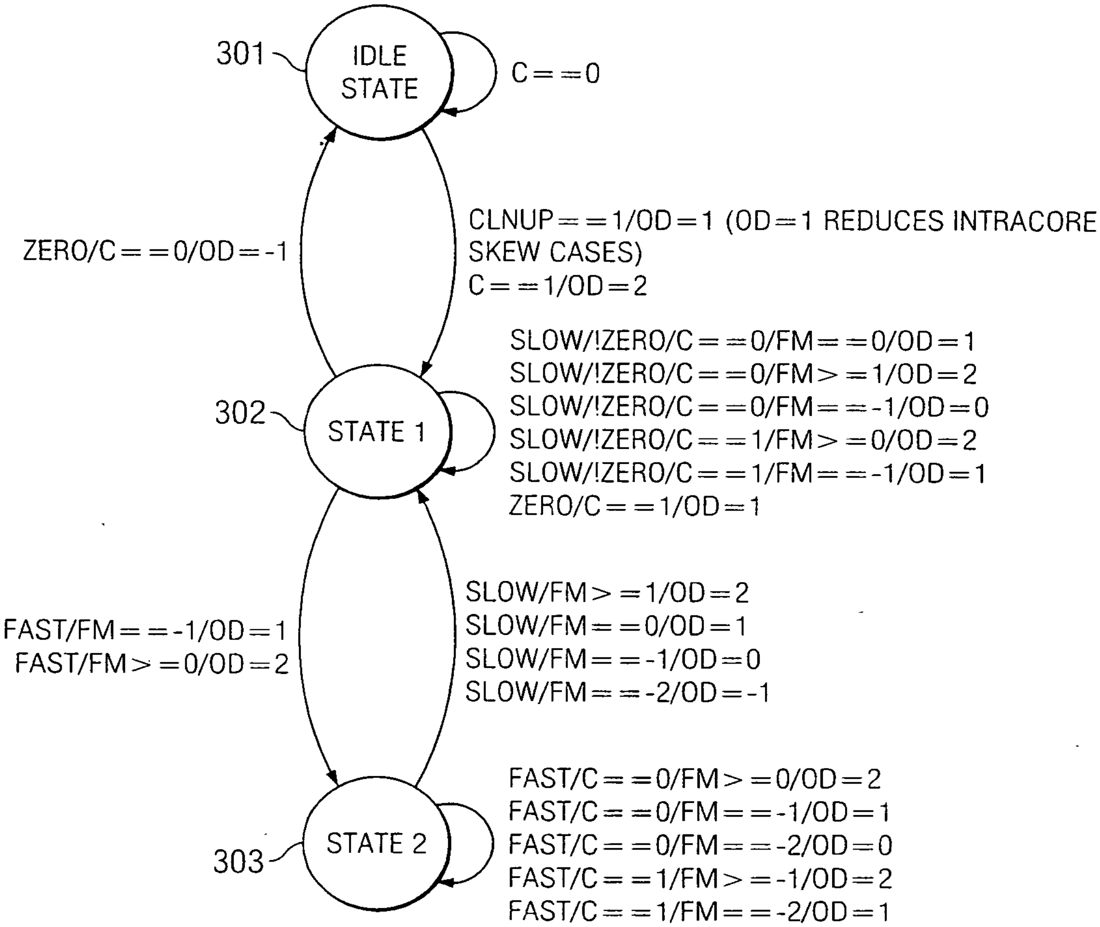

R
D
PHASE CONTROLLER
104
OVERDRIVE
PCSM
OUTPUT TO OTHER CONTROLLERS
OUTPUT TO ADJUST CLOCK
CORE
R
D
""C"" FILTER
201
R
D
PCSM
BLOCKED PREDICTION
202
103
205
HCSM
FREQUENCY MISMATCH
203
PHASE MISMATCH
204

FIG. 3


301
IDLE STATE
C==0
ZERO/C==0/OD=-1
CLNUP==1/OD=1 (OD=1 REDUCES INTRACORE SKEW CASES)
C==1/OD=2
SLOW/!ZERO/C==0/FM==0/OD=1
SLOW/!ZERO/C==0/FM>=1/OD=2
SLOW/!ZERO/C==0/FM==-1/OD=0
SLOW/!ZERO/C==1/FM>=0/OD=2
SLOW/!ZERO/C==1/FM==-1/OD=1
ZERO/C==1/OD=1
302
STATE 1
FAST/FM==-1/OD=1
FAST/FM>=0/OD=2
SLOW/FM>=1/OD=2
SLOW/FM==0/OD=1
SLOW/FM==-1/OD=0
SLOW/FM==-2/OD=-1
FAST/C==0/FM>=0/OD=2
FAST/C==0/FM==-1/OD=1
FAST/C==0/FM==-2/OD=0
FAST/C==1/FM>=-1/OD=2
FAST/C==1/FM==-2/OD=1
303
STATE 2